REMARKS

Entry of this Amendment in accordance with the provisions of 37 CFR §1.114 is respectfully requested.

This Amendment is in response to the Final Office Action dated June 13, 2006. The Amendment is being filed together with a Request for Continued Examination in order to obtain entry of this Amendment following the Final Rejection. By the present Amendment, the claims have been amended for clarification, as will be discussed below.

Briefly, by the present Amendment, a feature of the present invention is emphasized regarding the use of a CODEC circuit for compressing and uncompressing video data in conjunction with an arrangement for transferring data between a CPU (e.g., CPU 27 in Fig. 2) related to a first memory space (e.g., MAC in Fig. 4) and a peripheral LSI (e.g., PLSI 33 in Fig. 1) related to a second memory space (e.g., MAP in Fig. 4). A I/O bus (e.g., identified by the numeral 1 in Figs. 1 and 2) is connected to the peripheral LSI and related to the second memory space. Incidentally, it is noted that Fig. 1 provides a detailed illustration of the PLSI 33, which includes a flexible bus controller FBSC, which, itself, is shown in more detail in Fig. 3.

As shown in Fig. 1, the PLSI 33 includes a CODEC circuit GRP. The operation of the CODEC circuits in the data transfer operations are described, for example, on page 11 beginning with line 8. In particular, in the last paragraph on page 11 (beginning with line 17) an operation using the compression and decompression of the CODEC circuits GRP as described for transferring data from a memory MEM1 through the CPU bus 21 to the flexible BSC 22, from which the data

is transferred through the internal bus 4 to the CODEC circuits GRP. As noted beginning on page 11, line 22:

> "Then, the CODEC circuits GRP decode the video data and send the decoded data through the internal bus 4 to the flexible BCS 22. From the flexible BCS 22, the data is sent through the I/O bus 1 to the memory MEM 2. "

By virtue of the use of the CODEC circuit GRP as part of a bus master arrangement to compress video data before the video data is transferred from the I/O bus to the CPU bus 21, it is possible to prevent a large volume of video data from occupying the CPU bus 21 (as discussed, for example, on page 4, lines 23 and 24). In addition, the video data transfer without intermediation of the on-chip CPU is more advantageous in order to meet the need for high-speed data processing (as discussed, for example, on page 11, line 9 et seq.).

Reconsideration and removal of the 35 USC §112, second paragraph, rejection set forth on page 2 of the Office Action is respectfully requested. By the present Amendment, each of claims 9 and 10 has been amended to address the issues raised in the Office Action. Accordingly, reconsideration and removal of this rejection is respectfully requested.

Reconsideration and allowance of the amended independent claims 5, 7 and 15 and their respective dependent claims, including the new dependent claims 17-19, is respectfully requested.

By the present Amendment, each of the independent claims 5, 7 and 15 has been amended to specifically define a CODEC circuit which compresses and uncompresses video data, together with the operation of the CPU as a bus master and the feature:

> "wherein the uncompressed video data is transferred through the peripheral LSI from the CPU bus to the I/O bus after the CODEC circuit uncompresses the compressed video data; and
>
> wherein the compressed video data is transferred through the peripheral LSI from the I/O bus to the CPO bus after the CODEC circuit compresses the video data."

It is respectfully submitted that none of the cited references, including the primary reference to Takeda (USP 6,292,851) relied on in rejecting the previously submitted claims, teaches or suggests these claimed feature and operation of the CODEC circuit. As noted above, this arrangement prevents the undesirable large volume of video data from occupying the CPU bus, and permits higher speed data processing. Accordingly, reconsideration and allowance of the independent claims 5, 7 and 15 and their respective dependent claims, based upon these amended features is respectfully requested.

In addition, it is noted that the present independent claims 5, 7 and 15 and their dependent claims also define over the cited reference to Takeda by virtue of providing a CPU memory space (e.g., such as MAC in Fig. 4) and a peripheral memory space (e.g., such as MAP in Fig. 4) which are translated by an address translation circuit (e.g., ACON in Fig. 3). These circuit elements are specific hardware, unlike the arrangement in Takeda which translates addresses by software in response to an interrupt signal INT. See column 5, lines 22 and 23 and column 6, lines 10-42, as well as Figs. 7-9 of Takeda). Therefore, the present claims 5, 7, and 15 define a hardware structure which is completely lacking from the cited reference. When considered together with the above-noted CODEC circuit and the operation of the CODEC circuit defined in the claims, it is respectfully submitted that a combination is set forth in the independent claims 5, 7 and 15 and their respective

dependent claims, which is clearly neither taught nor suggested by the primary reference to Takeda, whether considered alone or in combination with the other cited prior art in this application. Therefore, reconsideration and allowance of claims 5-19 is respectfully requested for this reason as well.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 501.42810X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
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